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U.S. PATENT APPLICATION

for

METHOD OF IMPLANTING COPPER BARRIER MATERIAL TO IMPROVE ELECTRICAL PERFORMANCE

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CROSS REFERENCE TO RELATED APPLICATIONS

[0001] This application is related to U.S. Patent Application No. ____________, Attorney Docket No. 39153/474 (G1179), entitled METHOD OF INSERTING ALLOY ELEMENTS TO REDUCE COPPER DIFFUSION AND BULK DIFFUSION; U.S. Patent Application No. ____________, Attorney Docket No. 39153/519 (G1224), entitled USE OF MULTIPLE ELEMENTS TO FORM A ROBUST, ELECTROMIGRATION RESISTANT COPPER INTERCONNECT, U.S. Patent Application No. ____________, Attorney Docket No. 39153/457 (G1162), entitled METHOD OF USING TERNARY COPPER ALLOY TO OBTAIN A LOW RESISTANCE AND LARGE GRAIN SIZE INTERCONNECT; U.S. Patent Application No. ____________, Attorney Docket No. 39153/455 (G1160), entitled METHOD OF IMPLANTATION AFTER COPPER SEED DEPOSITION; and U.S. Patent Application No. ____________, Attorney Docket No. 39153/529 (G1234), entitled USE OF ULTR-LOW ENERGY ION IMPLANTATION (ULEII) TO FORM ALLOY LAYERS IN COPPER which are all assigned to the same assignee as this application.

FIELD OF THE INVENTION

[0002] The present invention relates generally to integrated circuits and methods of manufacturing integrated circuits. More particularly, the present invention relates to implanting copper barrier material to improve electrical performance.

BACKGROUND OF THE INVENTION

[0003] Semiconductor devices or integrated circuits (ICs) can include millions of devices, such as, transistors. Ultra-large scale integrated (ULSI) circuits can include complementary metal oxide semiconductor (CMOS) field effect transistors (FET). Despite the ability of conventional systems and processes to fabricate millions of IC devices on an IC, there is still a need to decrease the size of IC device features, and, thus, increase the number of devices on an IC. Nevertheless, there are many factors that make the continued miniaturization of ICs difficult. For example, as the size of vias (or pathways between integrated circuit layers used to electrically connect separate conductive layers) decreases, electrical resistance increases.

[0004] One way by which integrated circuit (IC) manufacturers have attempted to reduce via resistance as the via size decreases is reducing the thickness of the barrier material. For example, IC manufacturers can try to make the barrier material very thin at the bottom of the via. The thickness of the barrier material can be reduced by chemical vapor deposition (CVD) or advanced plasma vapor deposition (PVD) processes. Nevertheless, reducing the barrier thickness causes the barrier to become more permeable to copper (Cu) diffusion, which can adversely affect resistance to electromigration (EM).

[0005] FIGURE 1 illustrates a schematic cross-sectional view of a portion 100 of an integrated circuit including a copper layer 110, a via 120, and a copper layer 130. Via 120 and copper layer 130 are separated by a barrier layer 140. Copper layer 110 and via 120 can be one structure when formed in a dual in-laid process or, alternatively, two structures when formed in a single in-laid process. Barrier layer 140

inhibits diffusion of copper ions in general. Conventional barrier layers can include Tantalum Nitride (TaN).

[0006] Portion 100 also includes a dielectric layer 142 that is separated from copper layer 130 by an etch stop layer 144. Dielectric layer 142 can be oxide and etch stop layer 144 can be Silicon Nitride (SiN). Etch stop layer 144 prevents diffusion of copper from copper layer 130 into dielectric layer 142.

[0007] EM failures have been described by Stanley Wolf, Ph.D. in Silicon Processing for the VLSI Era, Vol. 2, pp. 264-65. Dr. Wolf explains that a positive divergence of the motion of the ions of a conductor leads to an accumulation of vacancies, forming a void in the metal. Such voids may ultimately grow to a size that results in open-circuit failure of the conductor line.

[0008] As discussed above, conventional systems have attempted to reduce the thickness of barrier layer 140 to reduce the resistance associated with via 120. However, this reduction in thickness can cause electromigration (EM) failures. FIGURE 2 illustrates portion 100 described with reference to FIGURE 1, further having an EM failure 145 in copper layer 130. FIGURE 3 illustrates portion 100 having an EM failure 155 in via 120. EM failures 145 and 155 can be due to a reduction in thickness of barrier layer 140.

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[0010] Thus, there is a need for a barrier that is more resistant to copper diffusion and thin enough for low via resistance. Further, there is a need for a method of implanting copper barrier material to improve electrical performance. Even further, there is a need for a method of enhancing barrier properties by implanting a heavy metal species to improve the permeability of the barrier layer to copper.

SUMMARY OF THE INVENTION

[0011] An exemplary embodiment is related to a method of fabricating an integrated circuit. This method can include forming a barrier material layer along lateral side walls and a bottom of a via that electrically connects a first conductive layer and a second conductive layer and implanting a metal into the barrier material layer. The implanted metal makes the barrier material layer more resistant to copper diffusion.

[0012] Another exemplary embodiment is related to a method of implanting copper barrier material to improve electrical performance in an integrated circuit fabrication process. This method can include providing a copper layer over an integrated circuit substrate, providing a barrier material at a bottom and sides of a via positioned over the copper layer to form a barrier material layer separating the via from the copper layer, amorphizing the barrier material layer, and providing a conductive layer over the via such that the via electrically connects the conductive layer to the copper layer. The metal species can make the barrier material layer more resistant to copper diffusion from the copper layer

[0013] Another exemplary embodiment is related to a method of forming a via in an integrated circuit. This method can include depositing a copper layer, depositing an etch stop layer over the copper

layer, depositing an insulating layer over the etch stop layer, forming an aperture in the insulating layer and the etch stop layer, forming an aperture in the insulating layer, providing a barrier material at a bottom and sides of the aperture form a barrier material layer providing separation from the copper layer, implanting a metal species into the barrier material layer, filling the aperture with a via material to form a via, and providing a conductive layer over the via such that the via electrically connects the conductive layer to the copper layer. The implanted metal species can make the barrier material layer more resistant to copper diffusion from the copper layer.

[0014] Other principle features and advantages of the invention will become apparent to those skilled in the art upon review of the following drawings, the detailed description, and the appended claims.

BRIEF DESCRIPTION OF THE DRAWINGS

[0015] The exemplary embodiments will hereafter be described with reference to the accompanying drawings, wherein like numerals denote like elements, and:

[0016] FIGURE 1 is a schematic cross-sectional view representation of a portion of an integrated circuit fabricated in accordance with prior art;

[0017] FIGURE 2 is a schematic cross-sectional view representation of the portion of the integrated circuit illustrated in FIGURE 1, showing an electromigration (EM) failure;

[0018] FIGURE 3 is a schematic cross-sectional view representation of the portion of the integrated circuit illustrated in FIGURE 1, showing an electromigration (EM) failure;

[0019] FIGURE 4 is a schematic cross-sectional view representation of a portion of an integrated circuit fabricated in accordance with an exemplary embodiment;

[0020] FIGURE 5 is a perspective cross-sectional view representation of a portion of the integrated circuit illustrated in FIGURE 4, showing a zero angle barrier layer implant; and

[0021] FIGURE 6 is a perspective cross-sectional view representation of a portion of the integrated circuit illustrated in FIGURE 4, showing a tilt angle barrier layer implant.

DETAILED DESCRIPTION OF THE EXEMPLARY EMBODIMENTS

[0022] With reference to FIGURE 4, a schematic cross-sectional view representation of a portion 400 of an integrated circuit (IC) includes a conductive layer 410, a via section 420, a copper layer 430, and a barrier layer 440. Portion 400 is preferably part of an ultra-large-scale integrated (ULSI) circuit having millions or more transistors. Portion 400 is manufactured as part of the IC on a semiconductor wafer, such as, a silicon wafer.

[0023] Portion 400 can also include a dielectric layer 442 that is separated from copper layer 430 by an etch stop layer 144. In an exemplary embodiment, dielectric layer 442 is an oxide material and etch stop layer 444 is Silicon Nitride (SiN) or other suitable material. Etch stop layer 444 prevents diffusion of copper from copper layer 430 into dielectric layer 442.

[0024] Conductive layer 410 can be a layer of any conductive material, such as, copper or another metal. Via section 420 can be made of a conductive material and serves to electrically connect

conductive layer 410 and copper layer 430. Copper layer 430 can be a layer of copper positioned in proximate location to via section 420. Copper layer 430 can be an alloy including copper (Cu). In an alternative embodiment, copper layer 430 is a stack of several layers.

[0025] Barrier layer 440 can be Tantalum (Ta), Titanium Nitride (TiN), Titanium Silicon Nitride (TiSiN), Tungsten Nitride (WNx), or other suitable material. In an exemplary embodiment, barrier layer 440 has a cross sectional thickness of 80 Angstroms. In other embodiments, barrier layer 440 can have dimensions as small as 10 Angstroms. The barrier properties of barrier layer 440 can be enhanced by the addition of an implant as described with reference to FIGURES 5 and 6.

[0026] In an exemplary method of fabricating portion 400, once copper layer 430 is created, etch stop layer 444 is deposited over copper layer 430 and dielectric layer 442 is deposited over etch stop layer 442. A resist layer is then deposited over dielectric layer 442 and is used in the patterning and etching of an aperture in dielectric layer 442 and etch stop layer 442 in the formation of via section 420. The resist layer is removed before depositing via material in via section 420 and depositing conductive layer 410.

[0027] Referring now to FIGURE 5, barrier layer 440 receives an implant 500 at a zero degree angle. Implant 500 can be a metal which upon implant with barrier layer 440 can make barrier layer 440 amorphous and more resistant to copper (Cu) diffusion. In an exemplary embodiment, implant 500 is a low dose, such as, $2e^{14}$ to $2e^{15}/cm^2$, and is implanted at an energy, such as, 0.5 to 5 keV.

[0028] Implant 500 can include heavy metals, such as, Hafnium (Hf), Lanthanum (La), Barium (Ba), Tin (Sn), and Zinc (Zn). Heavy metal species are particularly useful because they amorphise the

barrier at low energies. Implant 500 can also form an intermettallic with copper layer 430. An intermettallic is advantageous because diffusion will be reduced. In an exemplary embodiment, barrier layer 440 is Titanium Nitride (TiN) and implant 500 is Tin (Sn).

[0029] By providing implant 500 at a zero degree angle, a bottom 444 of via section 420 can be made more resistant to copper diffusion from copper layer 430. Advantageously, making the bottom of via section 420 more resistant to copper diffusion is good for electromigration.

[0030] Referring now to FIGURE 6, barrier layer 440 can also receive an implant 600 at a tilted angle. The angle of tilt can be 1 to 10 degrees with respect to bottom 444 of via section 430. Implant 600 can be a metal which upon implant with barrier layer 440 can make barrier layer 440 amorphous and more resistant to copper (Cu) diffusion. Due to the titled angle, barrier layer 440 at side walls 448 of via section 420 are made amorphous and resistant to copper diffusion. In an exemplary embodiment, implant 600 is a dose of, for example, $2e^{14}$ to $2e^{15}/cm^2$, and is implanted at an energy, such as, 0.5 to 5 keV.

[0031] One technique to achieve implantation of implant 600 at a titled angle is by rotating the integrated circuit wafer including portion 400. As such, an implanting device can be directed in one direction and, due to the rotation of the integrated circuit wafer, implant 600 can be provided along side walls 448 all around the aperture of via section 420.

[0032] Advantageously, making barrier layer 440 at side walls 448 of via section 420 more resistant to copper diffusion is good for BTS (biased thermal stressing) because the barrier is more resistant to copper diffusion. Thus, under BTS testing, copper is less likely to diffuse

from one line to an adjacent upper line. Further, implantation of the metal species on side walls 448 also improves line electromigration resistance because of the reduction in copper diffusion. Another advantage is that because the barrier is thinner, the line cross section is larger and, thus, the line resistance is lower.

[0033] While the exemplary embodiments illustrated in the figures and described above are presently preferred, it should be understood that these embodiments are offered by way of example only. Other embodiments may include, for example, different methods of implanting species. The invention is not limited to a particular embodiment, but extends to various modifications, combinations, and permutations that nevertheless fall within the scope and spirit of the appended claims.